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High through Put and Enhanced Quaternary Addition Using VLSI

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ABSTRACT: The main objective of this project is to design an enhanced Quaternary Signed Digit (QSD) adder with less propagation delay. Binary number system is easy to implement any arithmetic operations but they have their limitations in the area of circuit complexity and chip area which ultimately increases propagation delay of the circuit. To overcome these limitations QUATERNARY NUMBER SYSTEM is used. This number system decreases chip area about 25%. This project concentrates on the Quaternary Addition. Range of this numbers varies from -3 to 3. Quaternary addition involves carry free addition which reduces propagation delay.

KEYWORDS: Q.S.A, Latency, Binary addition,

1. INTRODUCTION

The major challenges in VLSI design are reducing the area of chip and increasing speed of the circuit. Reducing area can be achieved by optimization techniques and number of instructions executed per second increases as speed increases. The performance of a digital system depends upon performance of adders. Adders are also act as basic building blocks for all arithmetic circuits for example DSP processors. Binary adders are easy to implement because of logic levels involved in it '0' and '1', but they have their own limitations in the area of circuit complexity and chip area which ultimately increases propagation delay of the circuit. The drawback of binary adders can be reduced by increasing the range of the numbers used. Signed number system can be used for this purpose. Signed digit numbers allows redundancy of numbers which allow possibility of carry-free addition, but the signed digit number system allow limited carry propagation with some complex addition process which requires large for its implementation. To overcome all these limitations Multi Valued Logic number system is used. It has advantages in many areas as high density along with increasing the speed of operation. One such number system is QSD (Quaternary Signed Digit) number system.

QSD NUMBERS: Quaternary number system is four valued system, it is a base four number system. The QSD number set is { $\overline{3}$, $\overline{2}$, $\overline{1}$, 0, 1, 2, 3 } Where $\overline{3}$ represents -3, $\overline{2}$ represents -2 and $\overline{1}$ represents -1.Generalized QSD number D can be represented as

D= $\sum_{i=0}^{n-1} x^i 4^i$

Where x can be any value in the range of { $\overline{3}$, $\overline{2}$, $\overline{1}$, 0, 1, 2, 3 }. QSD negative number is the complement of QSD positive number.

Example: Advantages of QSD numbers are

1. Circuit complexity reduces in terms of transistor count and interconnections.
2. Occupies less space to store numbers of about 25% less when compared to Binary Signed Number system.
3. It uses parallelism and reduced gate complexity.
4. Computation speed increases.

ALGORITHM FOR QSD ADDER:

In QSD addition carry propagation chain is eliminated and hence propagation delay decreases which ultimately increases the system speed. The QSD addition range varies from 6 to +6 since the QSD number ranges from -3 to +3. Below table represents addition of two QSD digits.

TABLE1: Single digit addition result of QSD numbers.

Generalized QSD addition process is done in two steps.

STEP 1: Here intermediate sum and intermediate carry are generated from QSD input digits i.e. addend and augend .

STEP 2: In this step intermediate carry is left shifted by one bit and then combined with intermediate with sum. Decimal numbers from -3 to +3 are represented by one digit QSD number. If decimal number exceeds this range more than one bit of QSD number is required for its representation. For addition of two digits output range varies from -6 to +6 which requires two QSD digits for its representation.MSB represents sum bit and LSB bit represents carry bit. QSD numbers allow redundancy in their number representation i.e. same decimal number can be represented in more than one QSD number. One of such QSD number should be selected as QSD coded number

which prevents further carry rippling during addition. Rules that should be followed to choose a QSD coded number are

RULE 1: Intermediate Sum (IS) should be in the range of -2 to +2. (-2 and +2 are included)

IS= {-2,-1, 0, 1, 2}

RULE 2: Intermediate Carry (IC) should in the range of -1 to +1. (-1 and +1 are included)

IC= {-1, 0, 1}

Below table 2 represents the QSD code of a number.

TABLE 2: QSD coded numbers from -6 to +6

Sum in decimal	QSD representation	QSD coded number
-6	$\bar{2}\,2, 1\,\bar{2}$	$\bar{1}\,\bar{2}$
-5	$\bar{2}\,3, \bar{1}\,\bar{1}$	$\bar{1}\,\bar{1}$
-4	$\bar{1}\,0$	$\bar{1}\,0$
-3	$\bar{1}\,1, 0\,\bar{3}$	$\bar{1}\,1$
-2	$\bar{1}\,2, 0\,\bar{2}$	$0\,\bar{2}$
-1	$\bar{1}\,3, 0\,\bar{1}$	$0\,\bar{1}$
0	00	00
1	$01, 1\,\bar{3}$	01
2	$02, 1\,\bar{2}$	02
3	$03, 1\,\bar{1}$	$1\,\bar{1}$
4	10	10
5	$11, 2\,\bar{2}$	11
6	$12, 2\,\bar{3}$	12

	-3	-2	-1	0	1	2	3
-3	-6	-5	-4	-3	-2	-1	0
-2	-5	-4	-3	-2	-1	0	1
-1	-4	-3	-2	-1	0	1	2
0	-3	-2	-1	0	1	2	3
1	-2	-1	0	1	2	3	4
2	-1	0	1	2	3	4	5
3	0	1	2	3	4	5	6

The first column of the table represents decimal number, second column of the table shows the available multiple QSD representations of given decimal number and third column represents QSD coded number from above mentioned rules. Hence the addition of two QSD numbers is performed in two steps and further carry rippling is eliminated by using two rules for IC and IS. Addition process can be understood easily by using following examples

Ex1: ADD two numbers 40 and 40 in quaternary number system.

$40_{10} = 220_4$

:2 2 0

2 2 0

4 4 0

↓ ↓ ↓

10 10 00

IC: 110 IS: 000

STEP 2:

1 1 0 ⟶ IC shifted left bye one bit

0 0 0 ⟶ IS

1 1 0 0 ⟶ QSD RESULT

EXAMPLE 2:

ADD two numbers (negative example):130 and -200.

$130_{10} = 2002_4$

$-200_{10} = \bar{3}\,0\bar{2}0_4$

STEP 1:

2 0 0 2

$\bar{3}$ 0 $\bar{2}$ 0

$\bar{1}$ 0 $\bar{2}$ 2

↓ ↓ ↓ ↓

$0\bar{1}$ 00 $0\bar{2}$ 02

IC : 0000 IS : $\bar{1}0\bar{2}2$

STEP 2:

0 0 0 0 ⟶ IC shifted left by one bit

$\bar{1}$ 0 $\bar{2}$ 2 ⟶ IS

0 $\bar{1}$ 0 $\bar{2}$ 2 ⟶ QSD RESULT

↓

2. IMPLEMENTATION PROCEDURE

ADDITION PROCEDURE FOR SINGLE BIT:Addition of two single digit QSD numbers which ranges from -3 to +3 produces output in the range of -6 to +6. As this is out of range of input two bits are required to represent it. Lower significant bit serves as sum and most significant bit serves as carry bit. This addition process is done by converting the input into signed 2'scomplement

representation and all output combinations are tabulated in below table3.

INPUT				OUTPUT				
QSD		BINARY		DECIMAL	QSD		BINARY	
Ai	Bi	Ai	Bi	sum	Ci	Si	Ci	Si
3	3	011	011	6	1	2	001	010
3	2	011	010	5	1	1	001	001
2	3	010	011	5	1	1	001	001
3	1	011	001	4	1	0	001	000
1	3	001	011	4	1	0	001	000
2	2	010	010	4	1	0	001	000
1	2	001	010	3	1	-1	001	111
2	1	010	001	3	1	-1	001	111
3	0	011	000	3	1	-1	001	111
0	3	000	011	3	1	-1	001	111
1	1	001	001	2	0	2	000	010
0	2	000	010	2	0	2	000	010
2	0	010	000	2	0	2	000	010
3	-1	011	111	2	0	2	000	010
-1	3	111	011	2	0	2	000	010
0	1	000	001	1	0	1	000	001
1	0	001	000	1	0	1	000	001
2	-1	010	111	1	0	1	000	001
-1	2	111	010	1	0	1	000	001
3	-2	011	110	1	0	1	000	001
-2	3	110	011	1	0	1	000	001
0	0	000	000	0	0	0	000	000
1	-1	001	111	0	0	0	000	000
-1	1	111	001	0	0	0	000	000
2	-2	010	110	0	0	0	000	000
-2	2	110	010	0	0	0	000	000
-3	3	101	011	0	0	0	000	000
3	-3	011	101	0	0	0	000	000
0	-1	000	111	-1	0	-1	000	111
-1	0	111	000	-1	0	-1	000	111
-2	1	110	001	-1	0	-1	000	111
1	-2	001	110	-1	0	-1	000	111
-3	2	101	010	-1	0	-1	000	111
2	-3	010	101	-1	0	-1	000	111
-1	-1	111	111	-2	0	-2	000	110
0	-2	000	110	-2	0	-2	000	110
-2	0	110	000	-2	0	-2	000	110
-3	1	101	001	-2	0	-2	000	110
1	-3	001	101	-2	0	-2	000	110
-1	-2	111	110	-3	-1	1	111	001
-2	-1	110	111	-3	-1	1	111	001
-3	0	101	000	-3	-1	1	111	001
0	-3	000	101	-3	-1	1	111	001

TABLE 3: Addition result conversion from QSD to signed binary 2's complement form for single digit QSD addition.

The minterms for the intermediate carry (IC_2, IC_1, IC_0) are:

$$IC_2 = a_2 b_2 (a_0 b_0 a_1 b_1) + (a_1+b_1)(a_2 b_0 + b_2 a_0)$$

$$IC_1 = a_2 b_2 (a_0 b_0 a_1 b_1) + (a_1+b_1)(a_2 b_0 + b_2 a_0)$$

$$IC_0 = IC_2 + a_2 b_2 (\overline{a_1 b_1 + b_1} b_0 + b_0 a_1 + b_1 a_0 + a_1 a_0)$$

Minterms for intermediate sums are:

$$IS_0 = a_0 \bar{b}_0 + \bar{a}_0 b_0$$

$$IS_1 = (a_1 \bar{b}_1 + \bar{a}_1 b_1)\, a_0 \bar{b}_0 + (a_1 \bar{b}_1 + \bar{a}_1 b_1)\, a_0 b_0$$

$$IS_2 = IS_0 (\bar{a}_1 b_1 + a_1 \bar{b}_1) + b_2 \bar{a}_1 \bar{b}_0 + \bar{a}_2 \bar{b}_1 a_0 + a_0 b_0 \bar{a}_1 \bar{b}_1 (a_2 + b_2)$$

The final sum which is carry free is generated from those outputs i.e. Intermediate carry (IC_2, IC_1, and IC_0) and Intermediate sum (IS_2, IS_1, and IS_0). Therefore it has six input and three output bits.

$$S_0 = IC_0 \overline{IS}_0 + IC_0 IS_0$$

$$S_1 = IC_1 \oplus IS_1 \oplus IC_0 IS_0$$

$$S_2 = IC_2 \oplus IS_1 \oplus (IC_1 IS_1 + (IC_1 \oplus IS_1) IC_0 IS_0)$$

Input augend A is represented by 3 variables A_0, A_1,A_2 and addend B is represented by 3 variables B_0 ,B_1, B_2. Outputs intermediate carry(IC), intermediate sum(IS) are represented by 3 variables IC_0, IC_1, IC_2 and IS_0 ,IS_1 ,IS_2 simultaneously. As IC can be represented using only 2 bits third bit is allotted same value as second bit. The six variable expressions for IC , IS and final sum can be resolved from above table using k-map reduction. Verilog code for IC, IS and SUM has been written and simulated using XILINX 14.7 simulator and then synthesized using SYNPOSIS DESIGN COMPILER.

3. ADDITION PROCEDURE FOR MORE THAN 2 DIGITS:

N bit QSD addition is done in 2 steps. First step IC and IS are generated and in second step IC is left shifted by one digit and then added with IS using sum equations solved from above table. Further carry rippling is eliminated by two rules as mentioned above in section 2. These limitations over IC and IS restricts sum from overflow and therefore final result will be carry free. respectively. As illustrated in this proposed decomposition method achieves higher printability because of the following

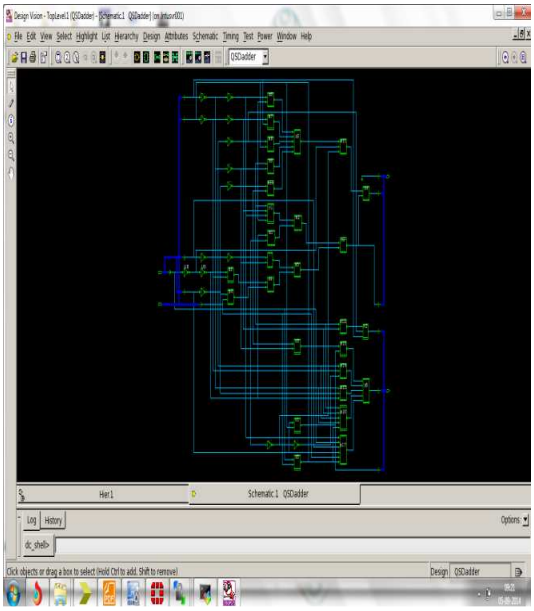
4. RESULTS

In this paper low power QSD ADDER unit is simulated using Modelsim and synthesizeed using XILINX Design Compiler in
Operating Condition Name: TYPICAL
Wire Loading Model Mode: top.

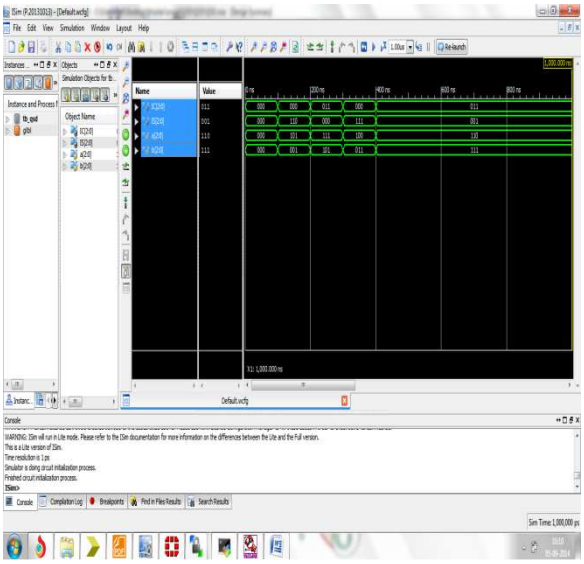
-3 -1	101 111	-4	-1 0	111 000
-1 -3	111 101	-4	-1 0	111 000
2 -2	110 110	-4	-1 0	111 000
-2 -3	101 110	-5	-1 -1	111 111
-3 -2	110 101	-5	-1 -1	111 111
-3 -3	101 101	-6	-1 -2	111 110

Simulation and layout designs are listed out as shown in below mentioned

Layout Synthesis Design Compiler For 1 Digit QSD Adder



OUTPUT OF SIMULATION



5. CONCLUSION

Finally, this project concludes that Quaternary signed digit adder for single digit addition is designed with low latency, power optimization and more accuracy. The dynamic power dissipation for designed project is 35.6781 at 13 GHz frequency. The delay of single digit adder is 0.73 ns. This design is simulated using MODELSIM and synthesized using Xilinx Design Compiler.

REFERENCES

[1] C. S. Lent, P. D. Tougaw, W. Porod, and G. H. Bernestein, "Quantum cellular automata," Nanotechnology, vol. 4, no. 1, pp. 49–57, 1993.

[2] M. T. Niemer and P. M. Kogge, "Problems in designing with QCAs: Layout = Timing," Int. J. Circuit Theory Appl., vol. 29, no. 1, pp. 49–62, 2001.

[3]Behrooz perhami "generalized signed digit number systems, a unifying frame work for redundant number reperesentation ".IEEE transactions on computers,vol 39,no.1,pp.89-98,January 19990.

[4]O. Ishizuka, A. Ohta, K. Tannno, Z. Tang, D. Handoko, "VLSI design of a quaternary multiplier with direct generation of partial products," Proceedings of the 27th International Symposium on Multiple-Valued Logic, pp. 169-174, 1997.

[5]A.A.S Awwal, Syed M. Munir, A.T.M. Shafiqul Khalid, Howard E. Michel and O. N. Garcia, "Multivalued Optical Parallel ComputationUsing An Optical Programmable Logic Array", Informatica, vol. 24, No. 4, pp. 467-473, 2000.

[6]F. Kharbash and G. M. Chaudhry, "Reliable Binary Signed Digit Number Adder Design", IEEE Computer Society Annual Symposium on VLSI, pp 479-484, 2007.

[7]John Moskal, Erdal Oruklu and Jafar Saniie, "Design and Synthesis of aCarry-Free Signed-Digit Decimal Adder", IEEE International symposium on Circuits and Systems, pp 1089-1092, 2007.

[8]Kai Hwang, "Computer Arithmetic Principles, Architecture and Design", ISBN 0-471-03496-7, John Wiley & Sons, 1979.

[9]P. K. Dakhole, D.G. Wakde, " Multi Digit Quaternary adder on Programmable Device : Design and verification",International Conference on Electronic Design, pp. 1-4, Dec 2008.

[10]Behrooz Parhami, "Carry-Free Addition of Recoded Binary Signed- Digit Numbers", IEEE Transactions on Computers, Vol. 37, No. 11, pp. 1470-1476, November 1988.

[11]Reena Rani, Neelam Sharma, L.K.Singh, "FPGA Implementation of Fast Adders using Quaternary Signed Digit Number System" IEEE proceedings of International Conference on Emerging Trends in Electronic and Photonic Devices & Systems (ELECTRO-2009), pp 132-